**Department of Computer Science & Engineering**

**University of Asia Pacific (UAP)**

**Program: B.Sc. in Computer Science and Engineering**

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| **Final Examination** | **Fall 2020** | **4TH Year 2ND Semester** | | |
| **Course Code: CSE 457** | **Course Title: Design and Testing of VLSI Circuit** | | | **Credits: 3** |
| **Full Marks: 120\* (Written)** |  | | **Duration: 2 Hours** | |
| \* Total Marks of Final Examination: 150 (Written: 120 + Viva: 30) | | | | |
| **Instructions:**   1. There are **Four (4)** Questions. Answer all of them. All questions are of equal value. Part marks are shown in the margins. 2. Non-programmable calculators are allowed. | | | | |

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| **1.** | **a)** | Explain Lee’s algorithm.  Solve the following using lee’s algorithm:    Details of each steps should be explained. | **20** | CO2 |
|  | **b)** | Explain VLSI Circuit testing with a relevant diagram. | **10** | CO4 |
| **2.** |  | Consider the following circuit |  |  |
|  | **a)** | Draw the truth table of the circuit. | **5** | CO3 |
|  | **b)** | Design the CMOS equivalent circuit of this multiplexer. | **15** | CO2 |
|  | **c)** | As you know, a ring oscillator is constructed from an odd number of inverters. Estimate the frequency of a 33-stage ring oscillator. Consider YOUR ROLL as the delay in Picosecond.  For example, if your roll is 101, let delay be 101 Picosecond. | **10** | CO3 |
| **3.** |  | Consider the following circuit |  |  |
|  | | | | |
|  | **a)** | Briefly explain each part of the diagram.  (You need to draw this same diagram and clearly show the parts by arrow and write down details about them.) | **10** | CO3 |
|  | **b)** | Explain the working procedure with a diagram that shows which part is transparent and which part is opaque for the following clock and data input  Clock 0101  Data 1011  (You need to draw this same diagram and show transparent and opaque parts as the clock changes and data flows.) | **20** | CO3 |
| **4.** | **a)** | Show VLSI Design flow in a flow chart. | **10** | CO1 |
|  | **b)** | How to design your circuit so that no latch up occurs in your circuit in the event of an ESD? | **10** | CO3 |
|  | **c)** | What are the three key regions of a bathtub curve in reliability testing. Briefly state the reason behind their identification name. | **10** | CO1 |
|  |  | **OR** |  |  |
|  | **a)** | Draw the Y-chart diagram used in VLSI Design. | **10** | CO1 |
|  | **b)** | Why is an FPGA popular from an engineering design point of view? | **10** | CO3 |
|  | **c)** | Draw a simple diagram of FPGA architecture and briefly state how does a FPGA runs its operation. | **10** | CO1 |